CONTENT ADDRESSABLE MEMORY (CAM) DEVICES HAVING SOFT PRIORITY RESOLUTION CIRCUITS THEREIN AND METHODS OF OPERATING SAME

Abstract of the Disclosure

Content addressable memory (CAM) devices use both hard and soft priority techniques to allocate entries of different priority therein. The priorities of multiple CAM array blocks within the CAM device may be programmed before or as entries are loaded therein and may be reprogrammed during operation as the allocation of entries within the CAM device changes. The allocation of entries may change in response to additions or deletions of entries or as entries are reprioritized. The CAM devices include preferred priority resolution circuits that can resolve competing soft and hard priorities between multiple hit signals that are generated in response to a search operation. Such hit signals may be active to reflect the presence of at least one matching entry within a CAM array block. The resolution of which active hit signal has the highest overall priority among many can be used to facilitate the identification of the location (e.g., array address and row address) of a highest priority matching entry within the entire CAM device. A priority resolution circuit may also resolve competing hard priorities between two or more active hit signals having equivalent soft priority. This aspect of the priority resolution circuit is provided so that an active hit signal having a highest overall priority can be resolved whenever multiple CAM array blocks having the same soft priority are detected as having matching entries therein during a search operation.

#250084